

CLAIMS

What is claimed is:

- 5 1 An system on a chip netlist builder and verification computer system comprising:
- a user interface module for providing user friendly and convenient interfaces that facilitate easy entry and modification of user selections and parameters;
- 10 an expert system module for analyzing information supplied by said user module and automatically providing SoC building and verification data to said parameter application module;
- a parameter application module for applying parameters and developing command line strings based upon information received from said
- 15 user interface and said expert system;
- a chip level netlist generation module for automatically generating a chip level netlist based upon information received from said user interface module and said expert system module; and
- a verification module for generating a test bench and a logical
- 20 verification environment automatically including simulation models based upon information interpreted by said parameter application module.

2 The system on a chip netlist builder and verification computer system
of Claim 1 wherein said parameter application module creates directions
passed to other modules for execution.

5 3 The system on a chip netlist builder and verification computer system
of Claim 2 wherein said directions passed to other modules for execution
includes command lines.

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10 4 The system on a chip netlist builder and verification computer system
of Claim 1 wherein said SoC building and verification data provided by said
expert system is retrieved from a storage medium comprising a database of
building block circuit description files.

5 The system on a chip netlist builder and verification computer system
15 of Claim 1 wherein said chip level netlist generation module includes the
instantiation of internal IC devices and connections between the circuit blocks
for internal signals.

6 The system on a chip netlist builder and verification computer system
20 of Claim 1 wherein said user interface module generates user friendly
graphical user interfaces (GUIs) to facilitate selection of standardized circuit
blocks and parameterization of the selected circuit blocks.

7 In a computer system, an system on a chip netlist builder and verification computer method for facilitating creation and modification of IC designs utilizing existing circuit block designs, said method comprising the steps of:

- 5 providing a user friendly interface;
performing a parameter application process;
executing an expert system process;
implementing a chip level netlist generation process including core netlist and I/O pin netlists; and
10 verifying a system on a chip design automatically.

8 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:

- 15 assisting easy entry and modification of user selections and parameters;
presenting information regarding operations of said SoC netlist builder and verification method to a user; and
facilitating selection of standardized circuit blocks and parameterization of said selected circuit blocks.

20 9 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:

- creating an underlying structure list;
interpreting information and commands entered by a user; and

performing iterations required to generate an underlying structure list.

10 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:

- 5 determining which circuit block is selected by a user;
initializing a corresponding string;
processing operations for a circuit block a user has requested;
making an instance specific copy of the parameterizable command line string; and

10 updating a copy of the parameterizable command line string with user indicated parameters received for a particular instance.

11 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:

- 15 appending the circuit block attributes to other files; and
adding the gate count of a circuit block to a list of gate counts for an IC.

12 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:

- 20 generating an internal integration list associated with the circuit block;
and

utilizing said internal integration list in the processing of other routines included in an SoC netlist builder and verification computer method.

5 13 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the step of extracting circuit block descriptions from a storage location based upon the applied parameter information.

10 14 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:

creating an IC core level netlist in a desired location based on data structures that were populated in other routines of said SoC netlist builder and verification computer method; and

15 generating hardware description language VHDL or Verilog code that automatically performs the task of coupling circuit blocks together.

15 The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:

20 providing signal declarations;
producing required HDL assign statements in accordance with an assignment list; and

generating the HDL code that will instantiate each of those components based upon an instantiation list.

16 An system on a chip netlist builder and verification computer method comprising the steps of:

- receiving system specification information;
- 5 reusing standardized circuit block information;
- performing test bench integration;
- determining if a proposed circuit design passes a test;
- synthesizing circuit blocks; and
- creating a top level netlist.

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17 The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of receiving information associated with custom designed circuit blocks.

15 18 The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of writing a test.

19 The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of facilitating
20 communications from a user regarding circuit block selection and parameterization.

20 The system on a chip netlist builder and verification computer
method of Claim 16 in which system specification information is received via
a present invention GUI.

5 21 The system on a chip netlist builder and verification computer
method of Claim 16 further comprising the step of retrieving appropriate
information from storage sources.

22 The system on a chip netlist builder and verification computer
10 method of Claim 16 further comprising the steps of:
 generating hardware description language (HDL) files describing
connections between building block circuit descriptions; and
 creating external input and output hardware description language
 (HDL) files.

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